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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,985	02/22/2002	Reid James Riedlinger	10971429-1	9993

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,985	RIEDLINGER ET AL.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 09 April 2002 has been considered.

Please see the attached PTO-1449(s).

Drawings

2. The drawings filed on 22 February 2002 have been approved by the Examiner.

Specification

3. Applicant is requested to update any data (continuation serial number, patent number, etc...) concerning co-pending or related applications listed in the specification.

The status of the parent applications in paragraphs [0001], [0033], [0036], [0040], [0044], and [0052] should be updated as appropriate.

Claim Objections

4. Claims 19-20 are objected to because of the following informalities:

As per claim 19, lines 3 and 5, "cache" should be deleted.

As per claim 20, line 1, "B1" should be --19--.

As per claim 20, lines 2 and 3, "cache" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Mulla et al. (6,539,457).

As per claim 1, Mulla et al. teaches a cache memory system including an L1 cache memory which includes a plurality of banks. See column 10, lines 26-30, where figures 2A and 2B depict the internal elements of the L1 cache as set forth in column 5, lines 18-19. ("cache memory structure comprising multiple banks"). The L1 cache has 4 ports 107 ("plurality of access ports communicatively coupled to said cache memory structure"). See column 5, lines 43-44, and figure 1. The cache memory includes CAM logic 409 to determine bank conflicts ("circuitry operable to determine a bank conflict for pending access requests for said cache memory structure"). See column 10, lines 31-41. Based on determinations of the bank conflict check, an access will be blocked and out-of-order accesses occur using logic 507 ("circuitry operable to issue at least one access request to said cache memory structure out of the order in which it was requested, responsive to determination of said bank conflict"). See column 11, lines 5-14 (where the "other entries that can issue..." are out of order entries).

As per claim 2, Mulla et al. teaches that the conflict occurs between two accesses, e.g. access A and C in the example of figure 4A. See column 10, lines 51-53.

As per claim 3, Mulla et al. teaches a data queue 209, where just prior to inserting a new access into the queue, the bank number of the new access is compared to accesses stored in the queue ("pending accesses"). See column 10, lines 31-35.

As per claim 4, Mulla et al. teaches a conflict between pending access C and issued access A. See column 10, lines 50-55. In this example, access A will issue while access C remains pending (but still conflicts with access A until access A completes).

As per claim 5, Mulla et al. teaches a pipeline having a plurality of stages and performing loads and stores, where loads are read in stage L1M and stores are written in stage L1W ("one stage for performing a first type of access and a different stage for performing a second type of access"). See figure 5 and column 12, lines 31-35.

As per claims 6 and 7, Mulla et al. teaches that multiple access, loads ("second type") or stores ("first type"), cannot access the same bank at the same time. See column 10, lines 20-21.

As per claim 8, Mulla et al. teaches determining conflicting accesses in stages L1A, L1M, L1D, or L1C, and therefore determining non-conflicting accesses in those same stages. See column 12, lines 57-62. Loads are issued in LIM. See column 12, lines 21-35.

As per claim 9, Mulla et al. teaches a bank conflict between a pending access and an older access in the queue 209. See column 10, lines 33-35.

As per claim 10, Mulla et al. teaches potential bank conflicts between accesses entering the queue at the same time (i.e. in parallel). See column 10, lines 35-38.

As per claim 11, Mulla et al. teaches a cache memory system including an L1 cache memory which includes a plurality of banks (tag (address) and data). See column 10, lines 26-30, where figures 2A and 2B depict the internal elements of the L1 cache as set forth in column 5, lines 18-19. ("cache memory structure that comprises a plurality of address banks"). The L1 cache has 4 ports 107 and a data queue 209 storing address of data ("storing access requests for said cache memory structure in a pending request queue"). See column 10, lines 31-35. The cache memory includes CAM logic 409 to determine bank conflicts ("determining at least one access request in said pending request queue that has a bank conflict"). See column 10, lines 31-41. Based on determinations of the bank conflict check, an access will be blocked and out-of-order accesses occur using logic 507 ("determining at least one access request in said pending request queue that does not have a bank conflict...[that] is newer than the determined access request that has a bank conflict"). See column 11, lines 5-14. For example, Mulla et al. teaches an access A and access C which have a bank conflict. Access A is nominated for issuing. Since Access C cannot be issued, other, younger accesses will be allowed to issue ("nominating..."). See column 11, lines 5-14.

As per claim 12, Mulla et al. teaches that the cache has 4 ports 107 (column 5, lines 43-44, and figure 1) and that a plurality of entries that do not have conflicts can issue (see column 11, lines 5-6).

As per claim 13, Mulla et al. teaches issuing 4 requests from the ports to the L1 cache in each cycle (i.e. in parallel). See column 5, lines 42-44.

As per claim 14, Mulla et al. teaches that just prior to inserting a new access into the queue, the bank number of the new access is compared to accesses stored in the queue. See column 10, lines 31-35.

As per claim 15, Mulla et al. teaches a bank conflict between a pending access and an older access in the queue 209. See column 10, lines 33-35.

As per claim 16, Mulla et al. teaches that multiple access, loads ("second type") or stores ("first type"), cannot access the same bank at the same time. See column 10, lines 20-21.

As per claim 17, Mulla et al. teaches a pipeline having a plurality of stages and performing loads and stores, where loads are read in stage L1M and stores are written in stage L1W ("one stage for performing a first type of access and a different stage for performing a second type of access"). See figure 5 and column 12, lines 31-35.

As per claim 18, Mulla et al. teaches that multiple access, loads ("first type") or stores ("second type"), cannot access the same bank at the same time. See column 10, lines 20-21.

As per claim 19, Mulla et al. teaches a cache memory system including an L1 cache memory which includes a plurality of banks (tag (address) and data). See column 10, lines 26-30, where figures 2A and 2B depict the internal elements of the L1 cache as set forth in column 5, lines 18-19. ("memory structure comprising a plurality of address banks"). Mulla et al. teaches a data queue 209 ("means for queuing access requests"). See column 10, lines 31-35. The cache memory includes CAM logic 409 to determine bank conflicts ("means for determining"). See column 10, lines 31-41. Based on determinations of the bank conflict check, an access will be blocked and out-of-order accesses occur using logic 507 ("means for

nominating"). See column 11, lines 5-14 (where the "other entries that can issue..." are out of order entries).

As per claim 20, the L1 cache has 4 ports 107 ("plurality of access ports communicatively coupled to said cache memory structure"). See column 5, lines 43-44, and figure 1. Mulla et al. teaches issuing 4 requests from the ports to the L1 cache in each cycle (i.e. in parallel). See column 5, lines 42-44.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen et al. (6,393,512) teaches a bank conflict detection circuit.

Rangan (6,711,654) teaches bank conflict detection for an out-of-order cache including a queue and conflict correction unit.

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
July 15, 2004